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7,342,565 B2	10/762,082	03/11/2008	01/21/2004	4090	0553-0207.02

Respectfully Submitted,

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(12) **United States Patent**
Tanaka

(10) **Patent No.: US 7,342,565 B2**
(45) **Date of Patent: Mar. 11, 2008**

(54) **DISPLAY DEVICE AND A DRIVER CIRCUIT THEREOF**

(75) Inventor: **Yukio Tanaka**, Kanagawa (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.** (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 720 days.

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Related U.S. Application Data

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G09G 3/36 (2006.01)

(52) **U.S. Cl.** 345/99; 345/211

(58) **Field of Classification Search** 345/99, 345/100, 211
See application file for complete search history.

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(57) **ABSTRACT**

To provide a driver circuit that is simple and possessing a small surface area. The driver circuit comprises a shift register circuit and a plurality of latch circuits. The shift register circuit is composed of a plurality of register circuits having a clocked inverter circuit and an inverter circuit connected in series. The plurality of digital data latch circuits has a first N-channel Tr and a second N-channel Tr of which the sources or the drains are connected in series, a P-channel Tr, and a data holding circuit. The clocked inverter circuit and the inverter circuit generate a timing signal on the basis of a clock signal and a start pulse to thereby feed the timing signal to the register circuit neighboring a register circuit and to a gate electrode of the first N-channel Tr and the P-channel Tr feeds a first electric voltage to the data holding circuit in accordance with a Res signal inputted to the gate electrode. The second N-channel Tr then takes in digital data on the basis of the timing signal to thereby output the digital data to the source or the drain of the first N-channel Tr. The timing signal outputted from the register circuit neighboring a register circuit is fed to the gate electrode of the first N-channel Tr.

(Continued)

32 Claims, 19 Drawing Sheets